Manonmaniam Sundaranar University,

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Tirunelveli - 627 012 Tamil Nadu, India

OPEN AND DISTANCE LEARNING(ODL) PROGRAMMES

(FOR THOSE WHO JOINED THE PROGRAMMES FROM THE ACADEMIC YEAR 2023–2024)

III YEAR

B.Sc. Physics

Course Material

PP VI - JMPHP6 - ELECTRONICS

(Credits – 3)

Prepared

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Tirunelveli – 12

Contents:

1. V–I Characteristics of Junction Diode and Zener Diode

Aim

To study the forward and reverse bias characteristics of a P–N junction diode and a Zener diode, and to determine the knee voltage and Zener breakdown voltage.

Apparatus Required

P–N junction diode, Zener diode, DC regulated power supply, milliammeter, voltmeter, resistor, breadboard, and connecting wires.

Circuit Diagram

1.

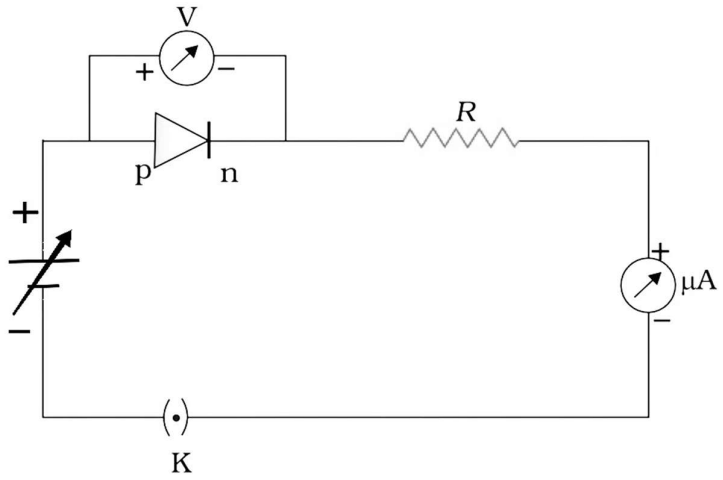


Figure 1.1 Circuit Diagram of P-N junction diode (Forward Biased)

2.

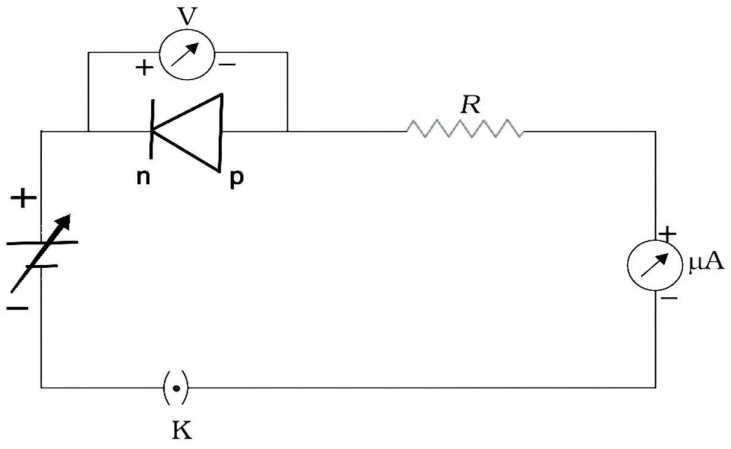


Figure 1.2 Circuit Diagram of P-N Junction Diode (Reverse Biased)

3.

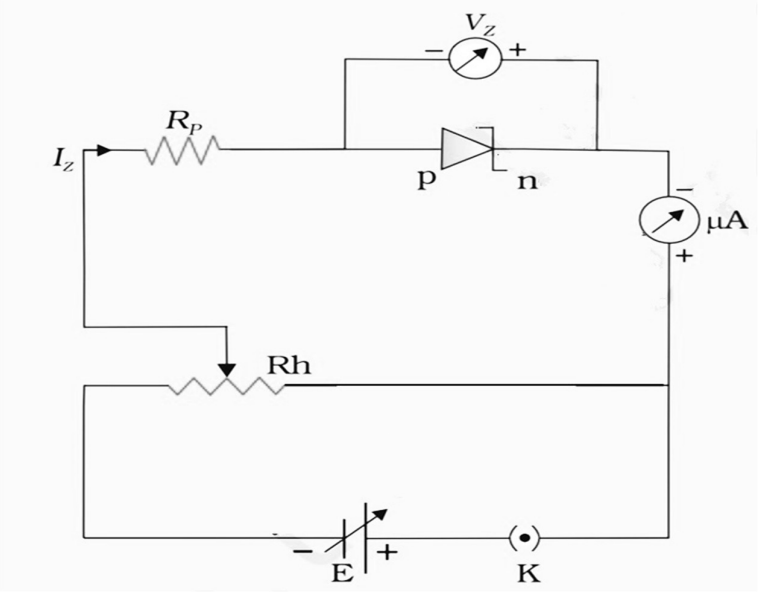


Figure 1.3 Circuit Diagram of Zener Diode in Reverse Bias (Reverse Breakdown Region)

Theory

A **P–N junction diode** allows current to flow in one direction (forward bias) and blocks it in the opposite direction (reverse bias).

In forward bias, the potential barrier decreases and current increases exponentially after the **knee voltage**.

In reverse bias, a small leakage current flows until the **breakdown region**, where current sharply increases.

For a **Zener diode**, when reverse-biased, it maintains a nearly constant voltage (the **Zener breakdown voltage**) across its terminals even if the current changes, hence used as a voltage regulator.

The current–voltage relation in the forward region is approximately:

$$\boldsymbol{I = I_0(e^{\frac{eV}{\eta kT}} - 1)}$$

where,

I_0 – saturation current,
η – ideality factor,
V – applied voltage,
k – Boltzmann constant (1.38×10^{-23} J/K),
T – absolute temperature.

Charge of an electron, e = 1.6×10^{-19} C

Procedure

A. For P–N Junction Diode

1. Connect the circuit for forward bias as shown.
2. Vary the input voltage from 0 to 1 V in steps of 0.1 V and note the corresponding current.
3. Reverse the diode connections for reverse bias.
4. Increase the reverse voltage gradually and record the reverse current up to the breakdown region.
5. Plot the **V–I characteristics** in both forward and reverse bias.

B. For Zener Diode

1. Connect the Zener diode in reverse bias as per circuit.
2. Vary the input voltage and record the corresponding current.
3. Plot the **V–I characteristic** and find the breakdown voltage.

Observation

(a) P–N Junction Diode – Forward Bias

S. No.	Voltage (V)	Current (mA)
1	0.1 (example)	0 (example)
2		
3		
4		
5		
6		

(b) P–N Junction Diode – Reverse Bias

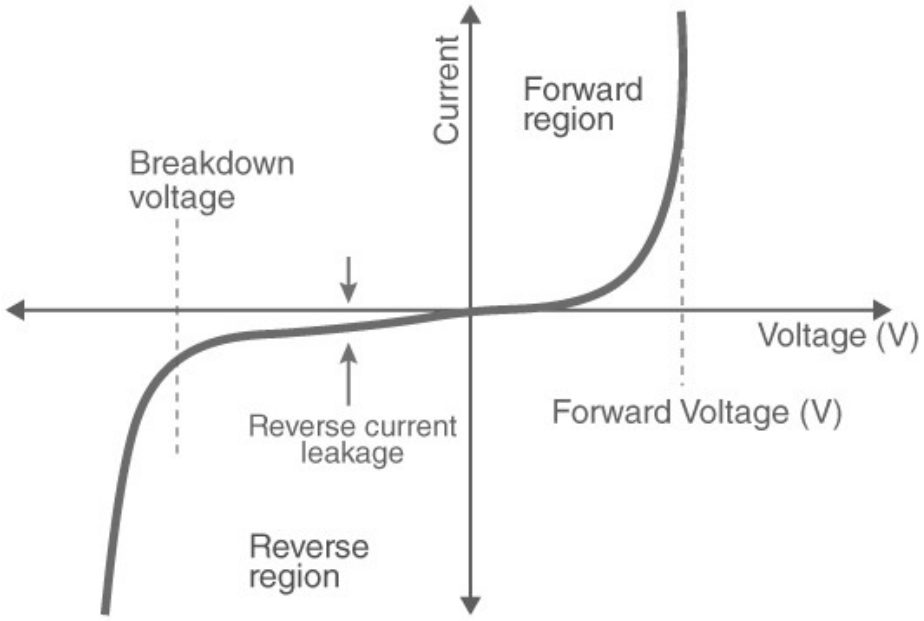
S. No.	Reverse Voltage (V)	Reverse Current (µA or nA)	Remarks
1	0.0	0	
2			
3			
4			
5			
6			
7			
8			
9			
10			*(Breakdown may start beyond this)*

(c) Zener Diode – Reverse Bias

S. No.	Voltage (V)	Current (mA)
1	2.0 (example)	0.1 (example)
2		
3		
4		
5		
6		

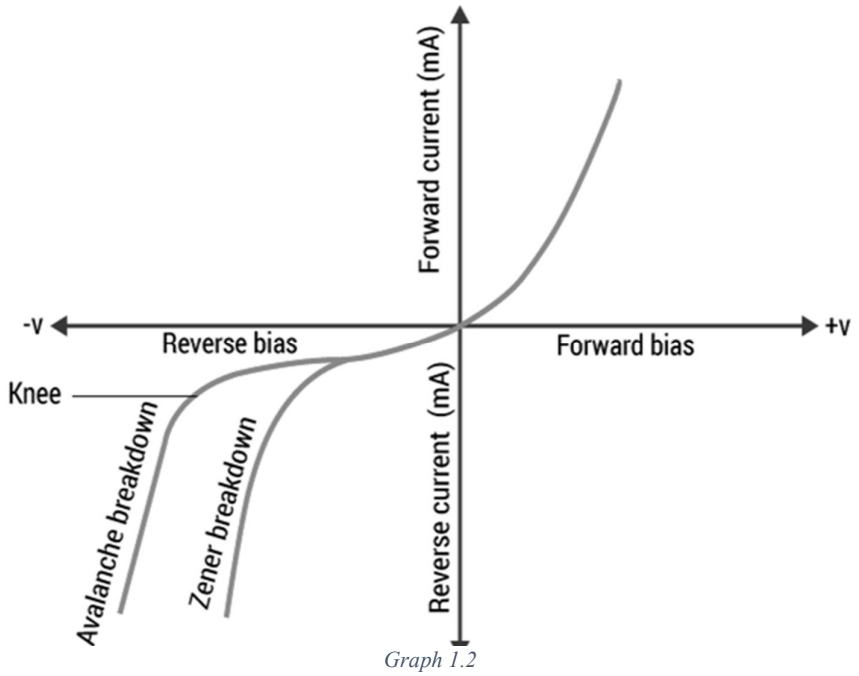
Graph

1. Plot **V–I curve** for the junction diode (forward and reverse).



Graph 1.1

2. Plot **Zener diode V–I curve** and mark the breakdown voltage (V_z).



Graph 1.2

Result

- **Knee Voltage (V_f)** of the junction diode = _____ V
- **Zener Breakdown Voltage (V_z)** = _____ V

Precautions

1. Connect the diode with correct polarity.
2. Do not exceed the maximum reverse voltage of the diode.
3. Increase voltage gradually while taking readings.
4. Note readings only after the circuit stabilizes.

Sources of Error

- Instrumental calibration errors.
- Voltage fluctuations in the power supply.
- Temperature variations affecting diode behaviour.

Discussion

1. What is the difference between a junction diode and a Zener diode?
2. What is knee voltage?
3. What happens to the current in reverse bias before breakdown?
4. Why is a Zener diode used as a voltage regulator?
5. What are the typical breakdown voltages for Zener diodes?

2. Zener Diode – Voltage Regulation using Bridge Rectifier

Aim

To study the voltage regulation characteristics of a **Zener diode** using a **bridge rectifier** circuit.

Apparatus Required

DC power supply (or step-down transformer with rectifier), Zener diode (5.1 V or 6.2 V), Resistors, Capacitor filter, Breadboard, Connecting wires, Voltmeter, Ammeter.

Circuit Diagram

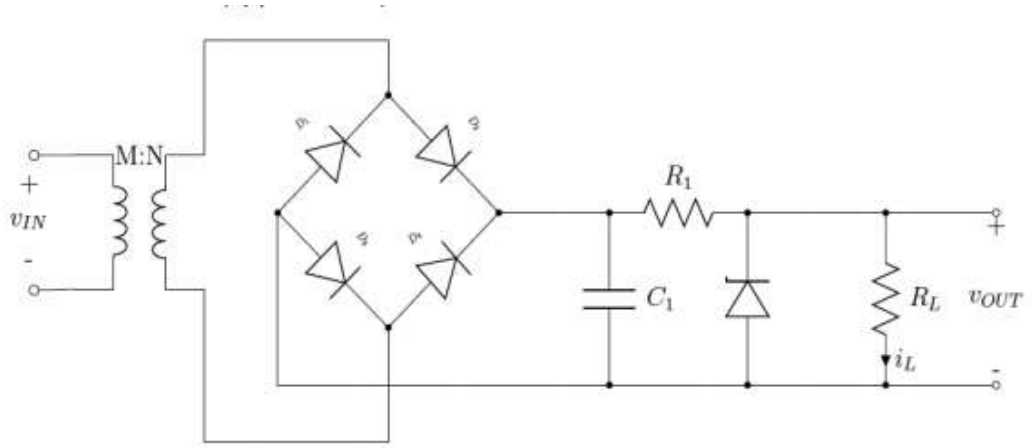


*Figure 2.1 voltage regulation by **Zener diode** using a **bridge rectifier** circuit*

Description

- The **AC supply** (230 V, 50 Hz) is connected to a **step-down transformer** (230 V/12 V).
- The **secondary output** of the transformer is given to a **bridge rectifier** made of four diodes (D_1, D_2, D_3, D_4).
- The **rectified output** passes through a **filter capacitor** to reduce ripple.
- The **Zener diode** is connected **in reverse bias** across the load resistor R_L.
- The **regulated DC output voltage** is measured across the load.

Theory

- A **Zener diode** when reverse biased beyond its **Zener breakdown voltage (Vz)** maintains a **constant voltage** across it, independent of the input voltage or load current, within limits.
- The **bridge rectifier** converts AC to pulsating DC, and with a filter capacitor, a smoother DC is obtained.
- This DC is then regulated by the Zener diode.

The **Zener diode voltage regulation equation** is:

$$V_{out} = V_Z \qquad \text{for } V_{in} > V_Z + I_Z R_Z$$

Procedure

1. Connect the circuit as per the diagram.
2. Vary the **input DC voltage** (rectifier output) using the transformer or variable power supply.
3. Measure the **output voltage across the Zener diode** for each input voltage.
4. Note the **input and output voltages** and **load current**.
5. Plot a graph between **output voltage (V_{out})** vs **input voltage (V_{in})**.

Observation

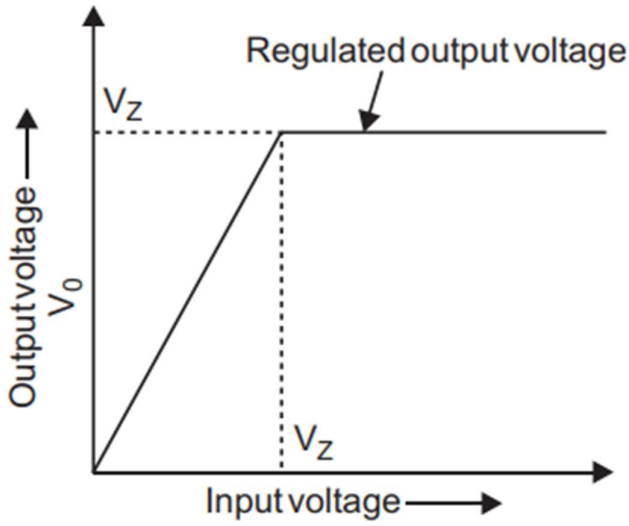
S. No.	Input Voltage (V_{in}) (V)	Load Voltage (V_{out}) (V)	Load Current (mA)
1	2 (example)		
2			
3			
4			
5			

*At a particular Voltage Regulation Starts and we get the Regulated voltage.

Graph

Plot **Output Voltage (V_{out})** on Y-axis vs **Input Voltage (V_{in})** on X-axis.

- The graph remains almost **constant** beyond the Zener breakdown region showing **voltage regulation**.



Graph 2.1

Result

The Zener diode maintains a nearly constant output voltage of ≈ ____ **V** for input voltages greater than the **Zener breakdown voltage**, thus acting as a **voltage regulator**.

Precautions

- Ensure correct polarity of the Zener diode (reverse bias for regulation).
- Use appropriate resistor values to limit current.
- Do not exceed the power ratings of diodes.
- Confirm proper diode connections in the bridge to prevent short circuits.

Discussion

- What is the principle of Zener diode voltage regulation?
- How does the series resistor protect the Zener diode?
- What is the difference between half-wave and full-wave rectification?
- Why is a bridge rectifier more efficient than a single diode rectifier?

3. Op-Amp – Adder and Subtractor

Aim

1. To design and study an **Op-Amp Adder (Inverting Summing Amplifier)**.
2. To design and study an **Op-Amp Subtractor (Differential Amplifier)**.

Apparatus Required

- Op-Amp IC 741
- DC Power Supply (±12 V or +12 V single supply)
- Resistors (10 kΩ, 22 kΩ, etc.)
- Breadboard and Connecting Wires
- Function Generator
- CRO / Digital Voltmeter

Circuit Diagram

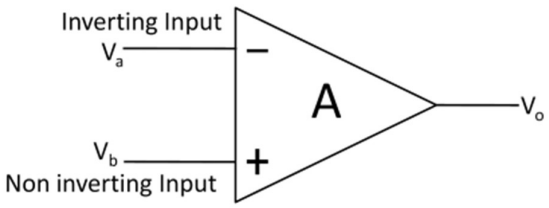


Figure 3.1

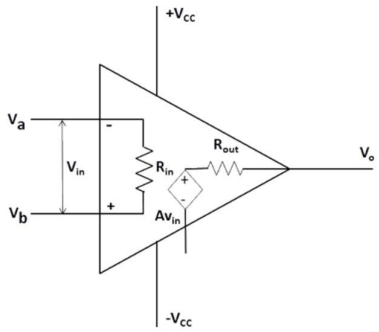


Figure 3.2

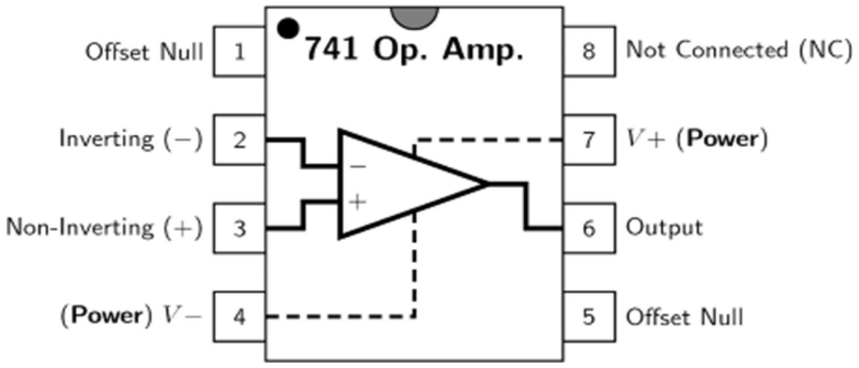


Figure 3.3

1. **Inverting Adder Circuit**
   - Non-inverting input (+) is grounded.
   - Inputs V_1, V_2 are applied through resistors R_1, R_2 to the inverting (−) terminal.
   - A feedback resistor R_f connects the output to the inverting input.

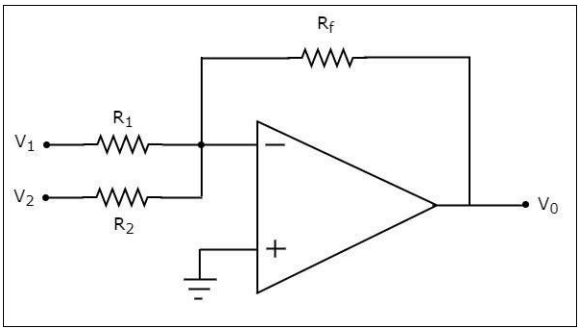


Figure 3.4

2. **Subtractor Circuit**
   - Two inputs V_1 and V_2 are applied to the op-amp through a resistor network.
   - $R_1 = R_3$ and $R_2 = R_4$ are used for unity gain differential operation.
   - Output voltage represents the difference between V_2 and V_1.

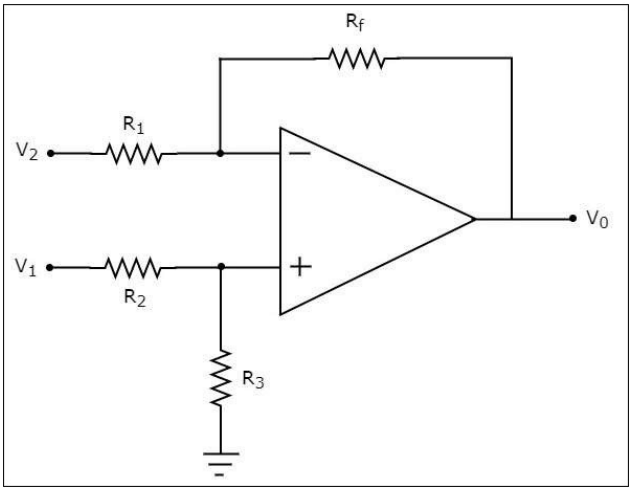


Figure 3.5

Theory

Inverting Adder (Summing Amplifier)

When multiple input voltages $V_1, V_2, V_3, \ldots$ are applied through resistors $R_1, R_2, R_3, \ldots$ to the inverting terminal of an op-amp, the output voltage is given by:

$$V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \cdots\right)$$

If all resistors are equal, $R_1 = R_2 = R_3 = R_f = R$, then,

$$V_{out} = -(V_1 + V_2 + V_3)$$

Subtractor (Differential Amplifier)

For the differential amplifier configuration, if $R_1 = R_3$ and $R_2 = R_4$, then,

$$V_{out} = \frac{R_2}{R_1}(V_2 - V_1)$$

When $R_1 = R_2 = R_3 = R_4$,

$$V_{out} = V_2 - V_1$$

Thus, the circuit amplifies the difference between two input voltages.

Procedure

Adder

1. Connect the circuit as per the diagram.
2. Keep all resistors equal (e.g., $R_1 = R_2 = R_f = 10\ k\Omega$).
3. Apply two input voltages $V_1$and V_2(e.g., 1 V and 0.5 V).
4. Measure the output voltage $V_{out}$for different sets of input voltages.
5. Record readings and compare with theoretical values.

Subtractor

1. Connect the differential amplifier circuit.
2. Use $R_1 = R_2 = R_3 = R_4 = 10\ k\Omega$.
3. Apply $V_1$and V_2as DC inputs.
4. Measure $V_{out}$for various combinations of $V_1$and V_2.
5. Record readings and verify $V_{out} = V_2 - V_1$.

Observation

1. Adder

S. No.	V_1 (V)	V_2 (V)	Theoretical V_{out} (V)	Measured V_{out} (V)
1	+1.0	+0.5	−1.5	
2				
3				

2. Subraction

S. No.	V_1 (V)	V_2 (V)	Theoretical V_{out} (V_2-V_1)	Measured V_{out} (V)
1	2.0	3.0	+1.0	
2				
3				

Result

The op-amp adder was verified to produce an output proportional to the sum of input voltages with an inversion of phase.

The op-amp subtractor was verified to produce an output equal to the difference between two input voltages.

Precautions

- Check op-amp pin configuration before powering.
- Use same resistor values to maintain accuracy.
- Do not exceed op-amp input or output voltage limits.
- Ensure proper grounding of the circuit.
- Use ±12 V supply for IC 741.

Discussion

1. What is the basic principle of an op-amp?
2. What is meant by virtual ground?
3. Why does the inverting adder produce a negative output?
4. Define CMRR.
5. How can the gain of the subtractor be adjusted?
6. What are the typical applications of summing and difference amplifiers?

4. Op-Amp Low Pass and High Pass Filters (Using IC 741)

Aim

To design and study the frequency response characteristics of

1. Active Low Pass Filter, and
2. Active High Pass Filter using Operational Amplifier IC 741.

Apparatus Required

- IC 741 operational amplifier
- Resistors: 10 kΩ, 100 kΩ
- Capacitors: 0.01 µF, 0.1 µF
- Function generator (0–1 MHz)
- Dual trace CRO
- DC regulated power supply (±12 V)
- Breadboard and connecting wires

Theory

An **Active Filter** uses an op-amp in combination with resistors and capacitors to amplify or attenuate specific frequency ranges.

(a) Low Pass Filter (LPF):

A low pass filter allows low-frequency signals to pass through and attenuates high-frequency signals beyond a certain **cutoff frequency (fc)**.

$$f_c = \frac{1}{2\pi RC}$$

For a non-inverting configuration,

$$A_v = 1 + \frac{R_f}{R_1}$$

- For $f < f_c$: Gain ≈ constant
- For $f > f_c$: Gain decreases at −20 dB/decade

(b) High Pass Filter (HPF)

A high pass filter allows high-frequency signals to pass through and attenuates low-frequency signals below the cutoff frequency f_c.

$$f_c = \frac{1}{2\pi RC}$$

The voltage gain is also given by:

$$A_v = 1 + \frac{R_f}{R_1}$$

- For $f < f_c$: Gain decreases
- For $f > f_c$: Gain ≈ constant

Circuit Diagrams

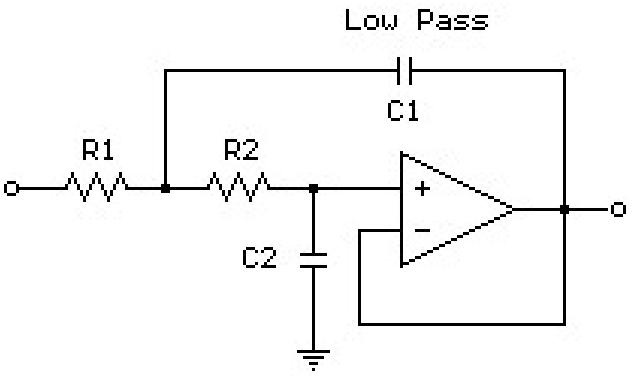


Figure 4.1

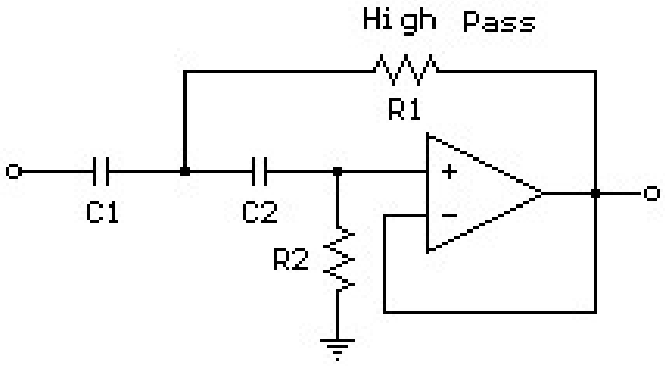


Figure 4.2

Procedure

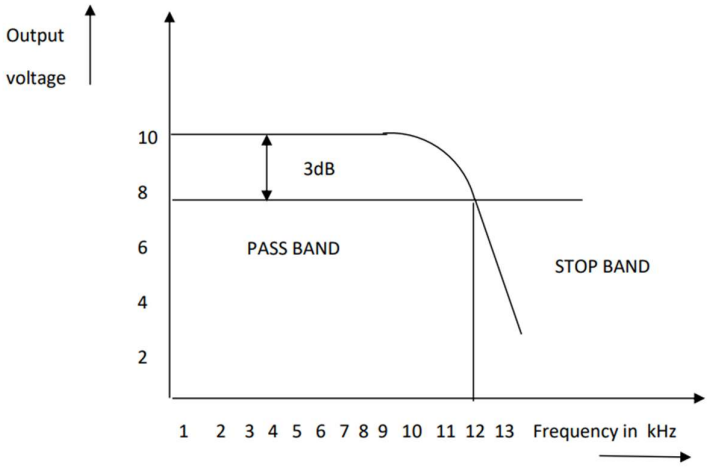
1. Connect the circuit as per the given circuit diagram.
2. Apply ±12 V dual DC supply to the op-amp (IC 741).
3. Give a 1 V (p-p) sinusoidal input signal from the function generator.
4. Vary the input frequency from 10 Hz to 1 MHz.
5. Observe and measure the output voltage at each frequency using the CRO.
6. Note down the input and output voltages.
7. Calculate the voltage gain $A_v = \frac{V_{out}}{V_{in}}$and gain in dB.
8. Plot a graph between Gain (dB) and log(frequency).
9. Determine the cutoff frequency (fc) from the −3 dB point.

Observation

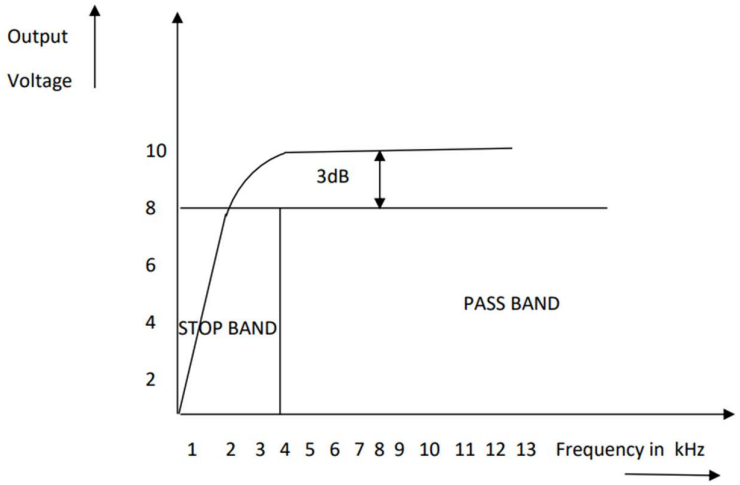
Frequency (Hz)	Input Voltage (V)	Output Voltage (V)	Gain (Vout/Vin)	Gain (dB)
100				
500				
1 k				
5 k				
10 k				

Model Graph

Plot **Voltage** versus **frequency** for both filters. The point at which the gain falls by **3 dB** from the maximum value gives the **cutoff frequency.**



Graph 4.1



Graph 4.2

Precautions:

1. Ensure correct polarity of ±12 V supply.
2. Avoid loose connections on the breadboard.
3. Use accurate resistor and capacitor values.
4. Keep input amplitude small to maintain linearity.

Result:

1. The cutoff frequency of the Low Pass Filter $f_{c1} =$ __Hz.
2. The cutoff frequency of the High Pass Filter $f_{c2} =$ __Hz.
3. The experimental values are in good agreement with theoretical results.

Viva Questions

- What is the effect of changing R and C on cutoff frequency?
- Explain the difference between passive and active filters.
- Why is buffering important in active filters?
- How does the op-amp improve filter performance compared to RC filters?

5. Characteristics of a Transistor in Common Emitter (CE) Mode

Aim

To study the input and output characteristics of an NPN (or PNP) transistor in **Common Emitter (CE) configuration** and to determine

1. Input resistance (Rin) and
2. Current gain (β or hFE).

Apparatus Required

- Transistor (e.g., BC107, 2N2222, or equivalent NPN type)
- Two variable DC power supplies
- Two voltmeters (0–1 V, 0–10 V)
- Two ammeters (0–10 mA, 0–100 μA)
- Resistors (as required)
- Breadboard and connecting wires

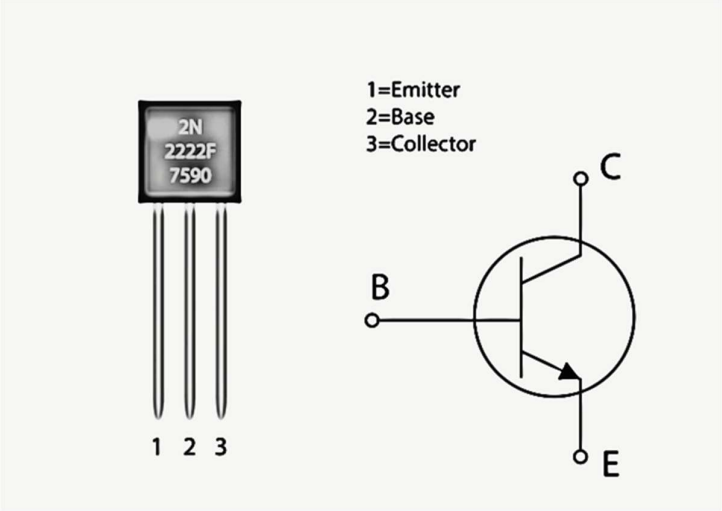


Figure 5.1 Transistor configuration

Circuit Diagram

- The **emitter** is common to both input (base–emitter circuit) and output (collector–emitter circuit).
- The **base** receives input current, and the **collector** is connected to the output circuit.

Connections

- Input: Between base and emitter → V_{BE}& I_B
- Output: Between collector and emitter → V_{CE}& I_C

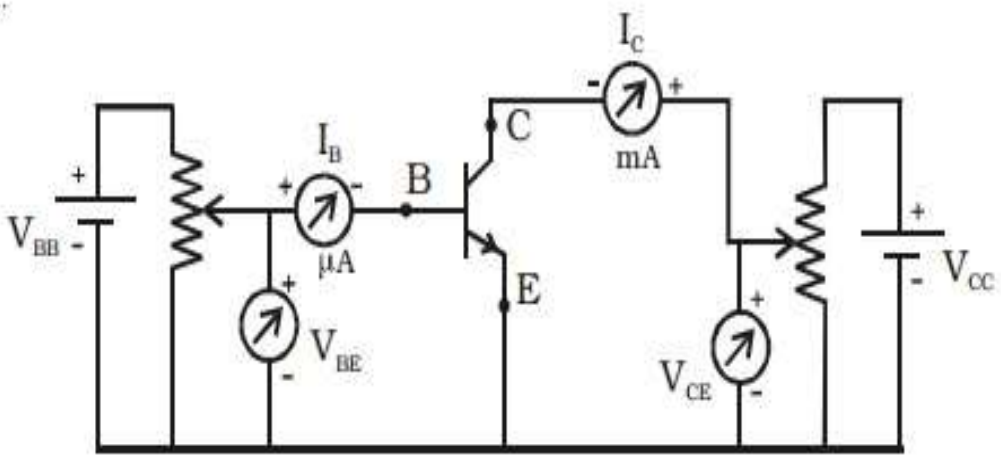


*Figure 5.2 transistor in **Common Emitter (CE) configuration***

Theory

In **CE configuration**,

- The input is a forward-biased base-emitter junction, and
- The output is a reverse-biased collector-base junction.

Thus, a small change in base current causes a large change in collector current giving high current and voltage gain.

Input Characteristics

The curve between base current (I_B) and base–emitter voltage (V_{BE}) at constant collector–emitter voltage (V_{CE}) shows the input behavior.

Output Characteristics

The curve between collector current (I_C) and collector–emitter voltage (V_{CE}) at constant base current (I_B) shows the output behavior.

Formulas

1. **Input Resistance:**

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} (\text{at constant } V_{CE})$$

2. **Current Gain:**

$$\beta = \frac{\Delta I_C}{\Delta I_B} (\text{at constant } V_{CE})$$

Procedure

(A) Input Characteristics

1. Connect the circuit as per the CE configuration.
2. Keep V_{CE} constant (say 2 V).
3. Vary the base–emitter voltage V_{BE} in small steps (0–1 V).
4. Note the corresponding base current I_B.
5. Plot a graph between **I_B (Y-axis)** and **V_{BE} (X-axis)**.

(B) Output Characteristics

1. Set a fixed base current I_B (say 20 µA).
2. Vary the collector-emitter voltage V_{CE} from 0 to 10 V.
3. Note the corresponding collector current I_C.
4. Repeat the same for different values of I_B (e.g., 20 µA, 40 µA, 60 µA...).
5. Plot a graph between **I_C (Y-axis)** and **V_{CE} (X-axis)** for each I_B.

(A) Input Characteristics

V_{BE} (V)	(I_B) (µA)	V_{CE} = constant
0.2		2 V
0.3		
0.4		
0.5		
0.6		
0.7		
0.8		

(B) Output Characteristics

V_{CE} (V)	I_C (mA) for I_B = 20 (µA)	I_C (mA) for I_B = 40 (µA)	I_C (mA) for I_B= 60 (µA)
0			
1			
2			
3			
4			
5			
6			
7			
8			

Graphs

1. **Input Characteristics:** I_B vs V_{BE}
   → Gives exponential behavior like a forward-biased diode.

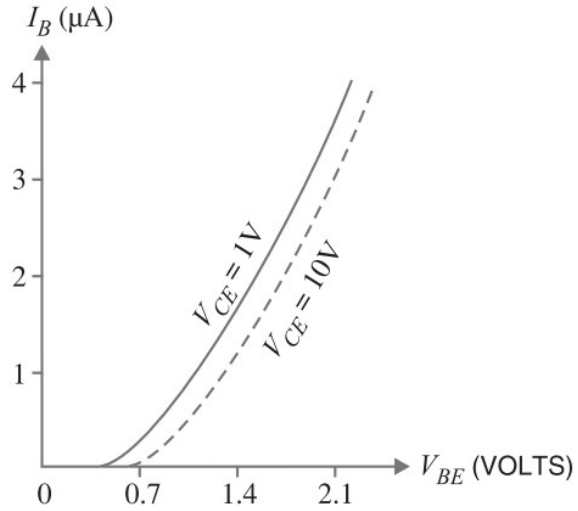


Figure 2

2. **Output Characteristics:** I_C vs V_{CE}
   → Shows active region, saturation region, and cut-off region.

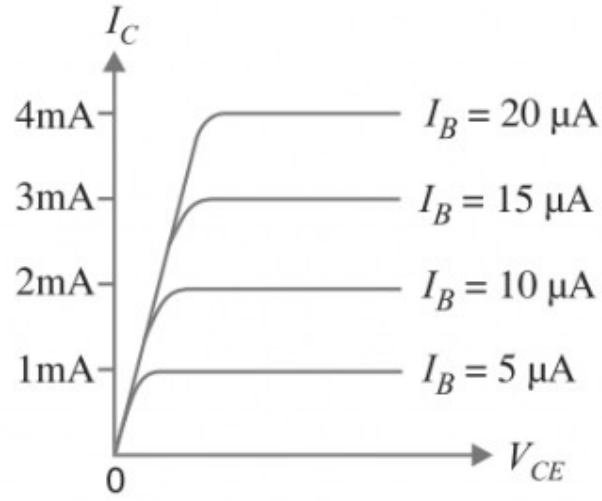


Figure 3

Calculations

From the graphs,

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} \text{(slope of input curve)}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} \text{(from output curves)}$$

Precautions

1. Do not exceed transistor's voltage and current ratings.
2. Make connections firmly to avoid fluctuations.
3. Increase voltages gradually and take readings carefully.
4. Transistor terminals (E, B, C) must be correctly identified.

Result

1. Input resistance $R_{in} =$ __ kΩ
2. Current gain $\beta =$ __

Discussion

- What are the three configurations of a transistor?
- Why is the common-emitter configuration most commonly used for amplification?
- Define current gain (β) in CE mode.
- What is the input and output impedance of a CE amplifier?
- What is the significance of the active region in the transistor characteristics?

6. Colpitts Oscillator Using Transistor

Aim

To construct and study the frequency of oscillation and waveform of a **Colpitts Oscillator** using a transistor in CE mode.

Apparatus Required

- Transistor BC107 or BC547
- Resistors: 1 kΩ, 10 kΩ, and 47 kΩ
- Capacitors: C_1 = 0.01 µF and C_2 = 0.001 µF
- Inductor: 1 mH
- DC Power Supply (9 V – 12 V)
- Breadboard or PCB
- Connecting wires
- Cathode Ray Oscilloscope (CRO)

Circuit Diagram

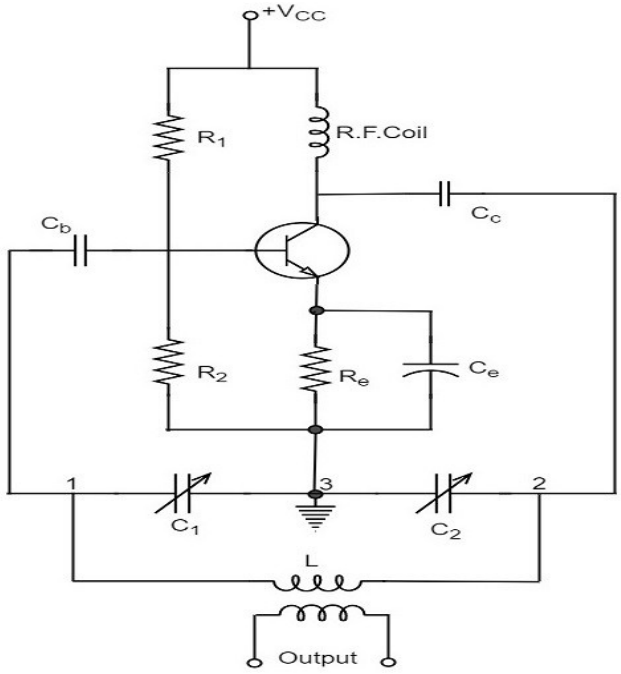


Figure 6.1 *Colpitts Oscillator using a transistor in CE mode*

Tank circuit (L, C_1, C_2) → connected between collector and emitter.
Feedback → through the capacitive divider (C_1–C_2).
Amplification → provided by the transistor (BC547).
Output → from the collector.

Theory

The **Colpitts oscillator** is an **LC type oscillator** that generates sinusoidal oscillations using an **inductor (L)** and **two capacitors (C_1 and C_2)** connected in a voltage divider configuration.

The feedback required for sustained oscillations is provided by this capacitive divider network.

The **transistor amplifier** compensates for losses in the circuit, ensuring continuous oscillations.

The oscillation frequency depends on the inductance and the equivalent capacitance of the tank circuit.

Formula for Frequency of Oscillation

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Where,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

Procedure

1. Connect the circuit as per the Colpitts oscillator circuit diagram.
2. Apply **9–12 V DC** power supply.
3. Observe the **output waveform** at the collector terminal on the CRO.
4. Note the **frequency of oscillation** from the waveform.
5. Compare the experimental frequency with the theoretical value using the formula.

Observation Table

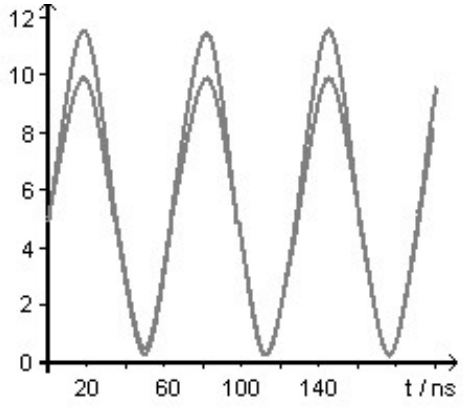
S. No.	C_1 (µF)	C_2 (µF)	L (mH)	Theoretical f (kHz)	Observed f (kHz)	Waveform Shape
1	0.01	0.001	1			Sinusoidal
2	0.02	0.002	1			Sinusoidal

Calculation

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Output on CRO



Graph 6.1 *Time in ns vs Output Voltage (Theoretical and experimental waveforms)*

Result

The Colpitts oscillator circuit was successfully constructed. A **sinusoidal output waveform** was observed on the CRO, and the **measured frequency** was found to be approximately equal to the theoretical value.

Discussion

1. What is the basic principle of the Colpitts oscillator?
2. Why are two capacitors used in this oscillator?
3. What is the role of the transistor in the circuit?
4. Write the expression for the frequency of oscillation.
5. Mention any two practical applications of the Colpitts oscillator.

7. Characteristics of a Field Effect Transistor (FET)

Aim

To study the output (drain) and transfer characteristics of a Junction Field Effect Transistor (JFET) in common-source configuration.

Apparatus Required

- N-channel JFET (e.g., BF W-10)
- DC power supplies (0–15V for drain and 0–3V for gate bias)
- Resistors as required
- Milliammeter and voltmeter
- Connecting wires and breadboard

Circuit Diagram

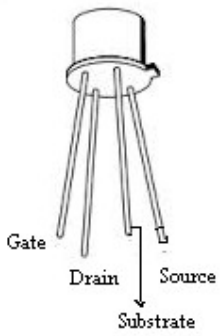


Figure 7.1 *pins in Field Effect Transistor*

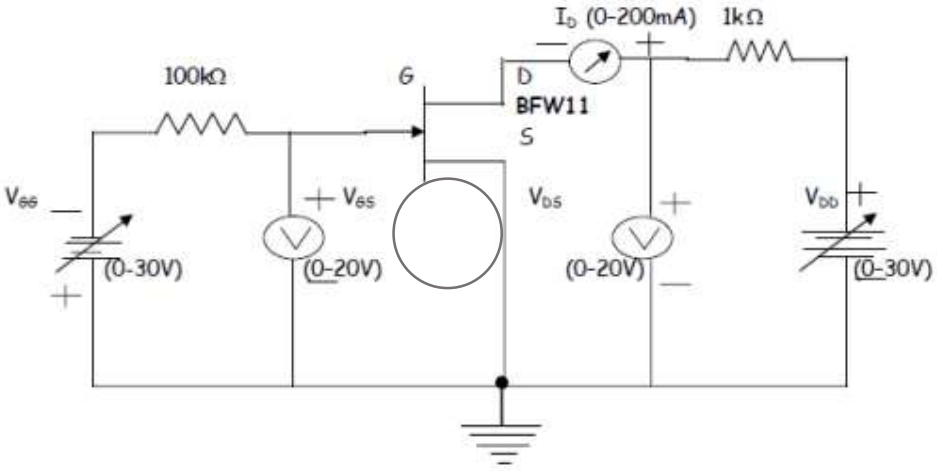


Figure 7.2 *Junction Field Effect Transistor (JFET) in common-source configuration*

Theory

- The FET is a unipolar device that controls current flow through a semiconductor channel using an electric field applied via the gate terminal.
- It has three terminals: gate (G), drain (D), and source (S).
- The current from drain to source (I_D) is controlled by the voltage between gate and source (V_{GS}) and the drain-to-source voltage (V_{DS}).
- FETs have high input impedance due to reverse-biased gate junctions.

Key Regions of Operation

- Ohmic (Linear) Region: Low V_{DS}, where I_D increases linearly with V_{DS}, behaving like a variable resistor.
- Active (Saturation) Region: I_D becomes relatively independent of V_{DS}, controlled primarily by V_{GS}.
- Breakdown Region: Excessive V_{DS} causes device damage.

Procedure

1. Set gate-source voltage $V_{GS} = 0V$. Vary V_{DS} from 0 to maximum (e.g. 15V). Measure and record drain current I_D. Plot I_D vs. V_{DS} (Output characteristic).
2. Repeat step 1 for different negative values of V_{GS} (e.g., -0.5V, -1V).
3. Fix V_{DS} at some value in saturation region (e.g., 5V).
4. Vary V_{GS} gradually from 0 to pinch-off voltage (V_P). Measure I_D. Plot I_D vs. V_{GS} (Transfer characteristic).

Key Formulas

- Drain current in active region:

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

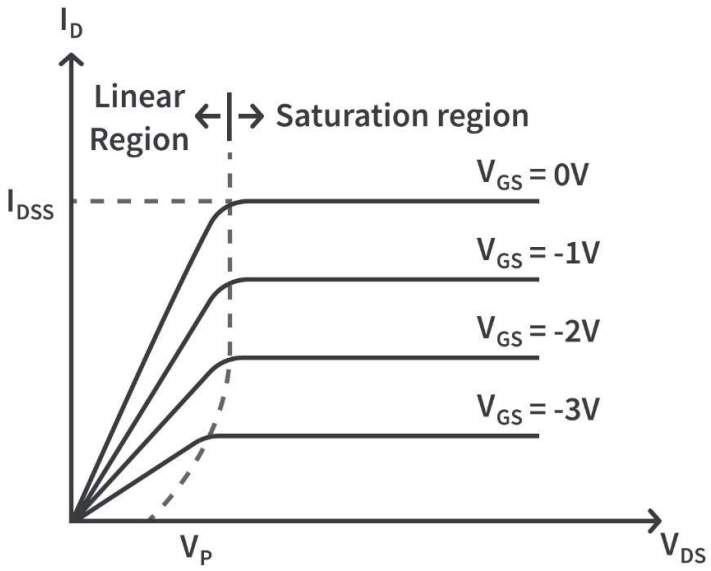
where

- I_{DSS} = drain current with gate shorted to source.
- V_P = pinch-off voltage (negative for n-channel JFET).
- Transconductance (gm):

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ at constant } V_{DS}$$

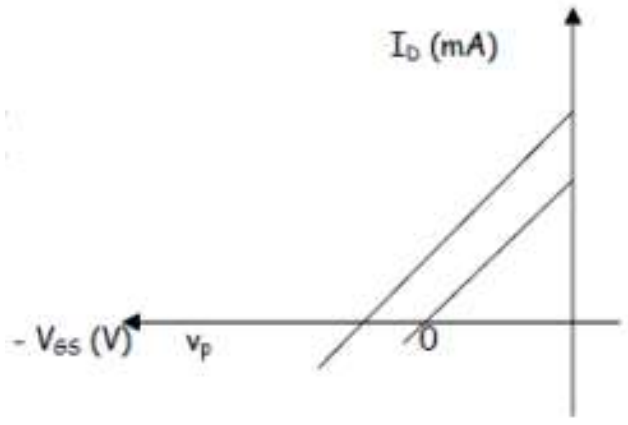
Observations and Graphs

1. Output Characteristics: Plot of I_D (drain current) vs. V_{DS} (drain-source voltage) for different fixed V_{GS} values.



Graph 7.1 *drain current vs drain source voltage*

2. Transfer Characteristics: Plot of I_D vs. V_{GS} at a fixed V_{DS}.



Graph 7.2 *drain current vs gate source voltage*

Precautions

- Ensure correct polarity for terminals.
- Avoid exceeding maximum ratings for voltage and current.
- Use high-impedance measuring instruments to prevent circuit loading.

Results

- Verified the FET operation in ohmic and saturation regions.
- Determined pinch-off voltage and drain current parameters.
- Observed high input impedance and voltage control of current.

Viva Questions

- What distinguishes a FET from a bipolar junction transistor?
- What role does the gate voltage play in controlling FET current?
- Explain the significance of pinch-off voltage.
- Why is FET preferred in high-input impedance applications?

8. Astable Multivibrator using 555 Timer

Aim

To design and study an **astable multivibrator** circuit using the **IC 555 timer** and to determine its **frequency** and **duty cycle**.

Apparatus Required

- IC 555 Timer
- Resistors R_1, R_2
- Capacitor C
- Breadboard
- DC Power Supply (5–12 V)
- Connecting wires
- CRO (Cathode Ray Oscilloscope)

Circuit Diagram

Pin Configuration (IC 555)

1. Pin 1 – GND: Ground (0 V reference).
2. Pin 2 – TRIG: Starts timing (< 1/3 V_{cc}).
3. Pin 3 – OUT: Output terminal.
4. Pin 4 – RESET: Active low; usually tied to V_{cc}.
5. Pin 5 – CTRL: Control voltage (bypass 0.01 µF to GND).
6. Pin 6 – THR: Ends timing (> 2/3 V_{cc}).
7. Pin 7 – DISCH: Discharges capacitor.
8. Pin 8 – V_{cc}: Supply voltage (+5 V – 15 V).

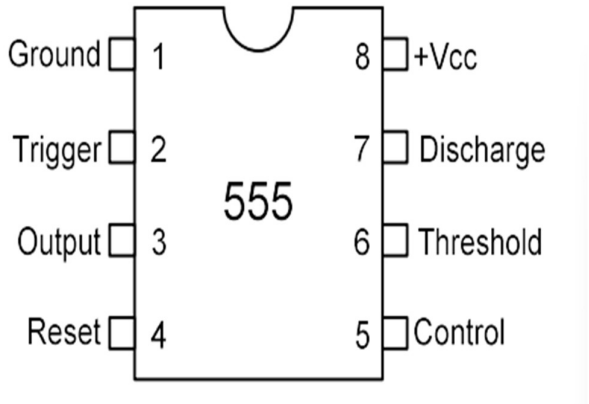


Figure 8.1 *pin configuration of 555 IC Timer*

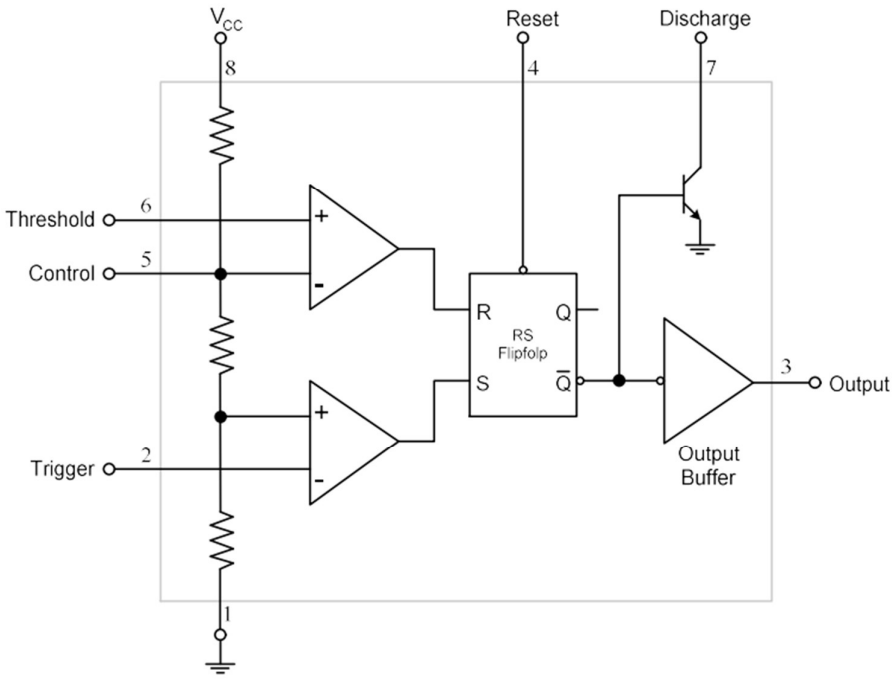


Figure 8.2 *Equivalent circuit diagram of 555 IC timer*

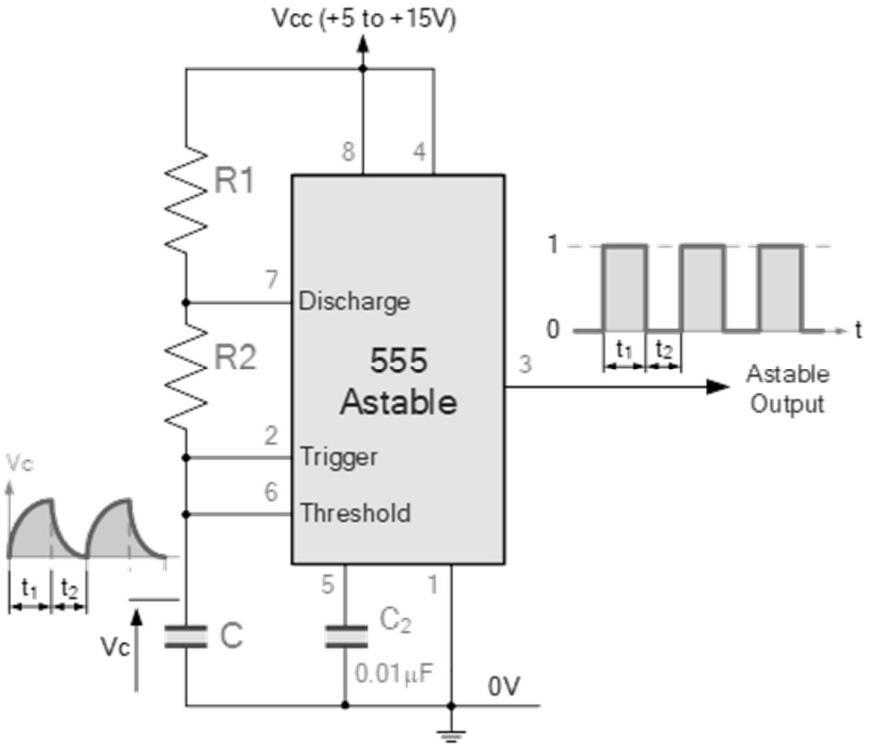


Figure 8.3 *Astable multivibrator circuit using the IC 555 timer*

Theory

The **IC 555 Timer** can be operated in three modes:

1. **Monostable mode** – one-shot pulse generator
2. **Astable mode** – free-running oscillator
3. **Bistable mode** – flip-flop operation

In astable mode, the circuit continuously switches between its high and low states without any external triggering. Hence, it is called a *free-running multivibrator*.

Working Principle

- When the 555 is connected in astable mode, the capacitor C charges through both R_1 and R_2, and discharges only through R_2.
- This continuous charge–discharge action produces a square wave output at pin 3.

Formulas

1. **Time period (T):**

$$T = 0.693(R_1 + 2R_2)C$$

2. **Frequency (f):**

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

3. **Duty Cycle (D):**

$$D = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$$

Procedure

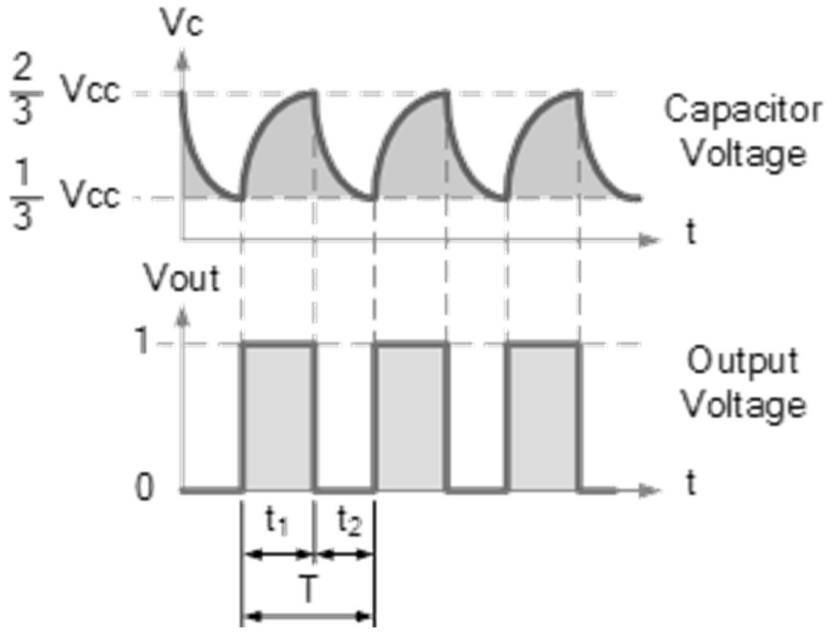
1. Connect the circuit as per the circuit diagram.
2. Apply a suitable DC supply (typically 5 V).
3. Observe the output waveform at pin 3 on the CRO.
4. Measure the time period (T), frequency (f), and duty cycle (D).
5. Compare the experimental frequency with the calculated value using the formula.

Observation Table

S. No.	Resistor (R_1) (kΩ)	Resistor (R_2) (kΩ)	Capacitor (C) (μF)	Time period (T) (ms)	Frequency (f) (Hz)	Duty Cycle (%)	Waveform observed on CRO
1	1	10	0.01	—	—	—	Square wave
2							Square wave
3							Square wave

Graph

Plot the output waveform observed on CRO (a square wave).



Graph 8.1 Input and Output waveforms in CRO

Precautions

1. Ensure all connections are tight and correct before switching on the power supply.
2. Use proper values of R_1, R_2, and C as per the circuit design.
3. Connect the IC 555 in correct polarity — wrong pin connection may damage the IC.
4. Verify that the power supply voltage does not exceed the rated value of the IC (typically 5V–15V).
5. Observe the waveform carefully on the CRO by connecting the probe to the output pin (pin 3).
6. Discharge the capacitor before changing its value to avoid errors in readings.
7. Handle electronic components carefully to prevent electrostatic damage.

Result

The astable multivibrator using IC 555 was designed and the output frequency and duty cycle were determined as: f = _____ Hz, D = _____ %

Viva Questions

1. What is an astable multivibrator?
2. Why is the 555 timer called an astable multivibrator in this mode?
3. What are the main functions of resistors R_1 and R_2?
4. How does changing the capacitor C affect the output frequency?
5. What is the duty cycle, and how is it controlled?